Gate-All-Around Transistors at 3nm: Device Physics, Fabrication Challenges, and Beyond FinFET Scaling

Aditya Sinha & Nishant Choudhary

Abstract

This paper provides a comprehensive review of Gate-All-Around (GAA) transistors at the 3nm technology node, a critical inflection point in the semiconductor industry. While Moore's Law, as an empirical observation of exponential transistor scaling, faces fundamental physical and economic limits, the industry continues to advance through architectural innovation. The report first traces the evolution from planar to three-dimensional (3D) FinFETs, highlighting how the latter's scaling limitations at sub-5nm dimensions necessitated a new paradigm. It then delves into the superior device physics of GAA transistors, which achieve enhanced electrostatic control by fully wrapping the channel, thereby mitigating severe short-channel effects and quantum phenomena that degrade FinFET performance. A detailed analysis of the engineering challenges including advanced EUV lithography, complex inner spacer fabrication, and nanosheet stacking variability is presented. The paper also provides a comparative review of the divergent strategies of leading foundries: Samsung's early, high-risk transition to GAAFETs at 3nm versus TSMC's decision to push its refined FinFET architecture to its absolute limit. Finally, it explores the roadmap beyond 3nm, examining emerging architectures like Complementary FETs (CFETs), the potential of novel two-dimensional (2D) materials as a replacement for silicon, and the profound influence of artificial intelligence (AI) and machine learning (ML) workloads in driving system-level, rather than purely transistor-level, innovation.

Keyword

Gate-All-Around Transistors (GAAFETs), Nanosheet Field-Effect Transistors (NSFETs), 3nm Semiconductor Technology, Fabrication Challenges in Advanced Nodes, Complementary FETs (CFETs), 2D Materials for CMOS Scaling, Semiconductors, AI Hardware, VLSI Design

1. Introduction: The Continuation of Moore's Law in the Angstrom Era

The remarkable progress of the semiconductor industry over the past six decades has been guided by an empirical observation known as Moore's Law [3]. First articulated by Intel co-founder Gordon Moore in 1965, it predicted that the number of transistors on an integrated circuit would double approximately every two years with minimal increase in cost . This observation set the pace for the digital revolution, propelling continuous improvements in computing power and efficiency. However, delivering on Moore's Law today is fundamentally different from the methods of the mid-20th century [35]. The industry now confronts significant "roadblocks" including fundamental physical limits, escalating manufacturing costs, and material constraints . As transistors approach the atomic scale, quantum effects such as electron tunneling and leakage currents become pronounced, leading to higher energy consumption and heat generation . The cost and complexity of developing and manufacturing cutting-edge chips have skyrocketed, driven by technologies like extreme ultraviolet (EUV) lithography, which require highly specialized and expensive equipment . Furthermore, silicon, the traditional

material for semiconductors, is reaching its limits in terms of performance and scalability .

The most profound aspect of Moore's Law is its transformation from a mere projection of a trend into a motivating industry objective [35] . The sources reveal a continuous, relentless pursuit of this target by companies like Intel and their competitors. The breakthroughs in transistor design were not natural phenomena but a direct, costly, and strategic response to the imperative of maintaining the pace of a "law" that was never a law of nature, but a projection for the future that relied on innovation and technological advancement for its continued truth . This continuous need to innovate in response to emerging physical constraints provides the foundational narrative for the entire semiconductor industry.

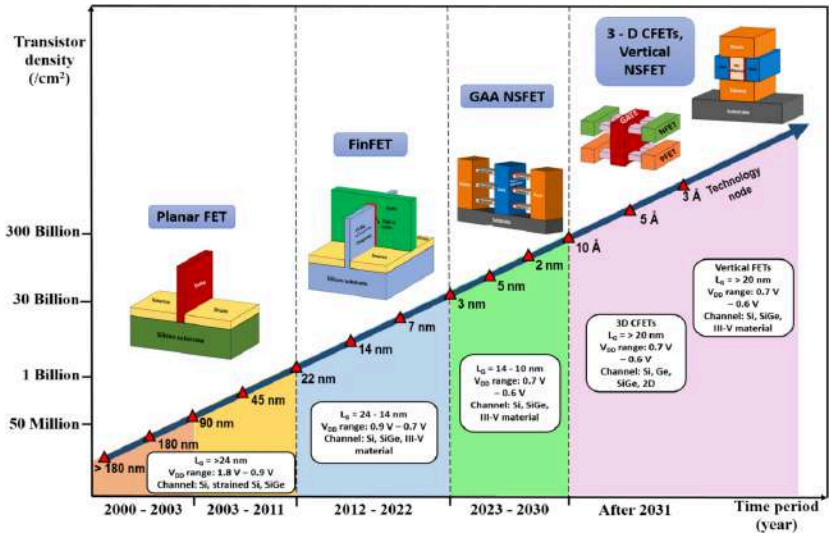

Figure 1. “Timeline/roadmap showing transistor scaling.” Credits: Springer Nature

1.2. The Three-Dimensional Evolution of Transistor Architectures

The transistor's architecture has evolved dramatically to meet the scaling demands imposed by Moore's Law [4]. The classical planar transistor, industrialized in the 1950s and 60s, was a two-dimensional structure where the gate modulated conductivity by acting on the top surface of the channel . As these planar transistors were downsized, they began to suffer from a variety of problems including gate leakage currents and short-channel effects .

The first major architectural leap was the transition to the Fin Field-Effect Transistor (FinFET) at the 22nm node [6] . This revolutionary design raised the channel above the plane of the silicon, shaping it into a vertical "fin" . The gate was then wrapped around three sides of this fin, dramatically increasing the gate's surface area and its control over the channel's current flow . This architectural innovation was a direct response to the limitations of planar designs, allowing for superior electrostatic control, reduced leakage, and enhanced drive current . The vertical geometry of FinFETs also enabled engineers to pack more transistors onto a chip, continuing the scaling trend [8] .

However, as dimensions continued to shrink, even FinFETs began to encounter limitations [6].

At the 5nm and 3nm nodes, the same problems of leakage currents and short-channel effects re-emerged . To further improve control, engineers developed the Gate-All-Around (GAA) transistor, which encloses the entire channel with the gate [16] . This is often achieved by replacing the vertical fin with a stack of horizontal nanosheets, allowing the gate to surround the channel on all four sides, a design that further reduces leakage and increases drive current . This evolution from planar to FinFET and now to GAA is not an arbitrary progression, but a direct, causal chain of innovation driven by the ever-increasing need for greater electrostatic control to overcome the physical realities of device scaling [39].

1.3. The 3nm Node: A Critical Inflection Point

The 3nm node marks a pivotal moment in semiconductor manufacturing, representing a strategic schism among the world's leading foundries. The evidence indicates that for many, this node is where FinFETs reached their fundamental limits [5]. According to one expert, at 3nm, "transistor development has hit a wall" for FinFETs, as the ceiling has been reached for key parameters like fin height and gate length [8] . This has created a "FinFET cliff," a metaphorical point where the marginal gains from scaling a FinFET-based process become prohibitively difficult to achieve, forcing a transition to a new architecture [8] .

This physical reality led to a strategic divergence among the major players . Samsung transitioned to its GAAFET technology, named Multi-Bridge-Channel FET (MBCFET), for its 3nm process (3GAE) [48]. This was a high-risk gamble to be the first to market with a new, complex architecture . In contrast, TSMC, the market leader, chose a more conservative approach, opting to push its mature FinFET architecture to its absolute limit for its 3nm node (N3/N3E) [8]. The fact that TSMC was able to successfully produce a 3nm FinFET node with significant performance, power, and area (PPA) improvements demonstrates the remarkable resilience of the FinFET design, but simultaneously confirms that the industry's ultimate move to GAA was inevitable for the next major node [8].

2. Methodology

This review was compiled and written as a focused, graduate-level synthesis of published and technical work on gate-all-around (GAA) transistors and related scaling strategies for ~3 nm technology and beyond. The goal of the methodology is transparency and reproducibility

Literature search and timeframe

A systematic search was performed covering the period **2008 - 2025** to capture the transition from FinFET-era literature through the first public GAA reports and the most recent industry and preprint material. Search keywords included combinations of: *“gate-all-around,” “GAAFET,” “nanosheet,” “nanosheet FET,” “CFET,” “3 nm,” “EUV,” “RibbonFET,” “SRAM scaling,” “nanosheet fabrication,”* and *“nanosheet variability.”* Primary sources were identified using technical databases and repositories (IEEE Xplore, IEDM/ISSCC/ VLSI/IEDM handouts, SPIE proceedings, MDPI journals, Nature Communications, AIP, arXiv, PubMed Central) and supplemented with foundry/industry technical releases (TSMC, Samsung, Intel), patents

(Google Patents / USPTO), and selected technical analyses (TechInsights, IEDM summaries). The final reference list for this review consists of **58** items spanning peer-reviewed papers, conference proceedings, preprints, technical reports, patents, and industry white papers.

Selection criteria and quality weighting
Sources were included if they provided (a) experimental device data or TCAD/simulation results relevant to GAA/nanosheet devices, (b) fabrication process descriptions (EUV, spacer, inner spacer, etch/deposition steps), (c) comparative analyses of transistor architectures, or (d) credible industry roadmaps and technical disclosures. Preference and interpretive weight were intentionally given to peer-reviewed journal articles and conference proceedings that report primary data or validated TCAD studies. Preprints and ResearchGate entries were used when they provided otherwise unavailable technical detail, but were explicitly checked against later peer-reviewed work where possible. News articles, blog posts, and press releases were retained only for factual context (e.g., product launch dates, foundry announcements) and are not the basis for device physics claims.

Data extraction and synthesis
From each primary technical source, the review extracted technical metrics and qualitative findings that directly inform scaling and performance (e.g., threshold voltage behavior, subthreshold swing, DIBL, drive current, parasitic capacitances, reported PPA improvements, process steps affecting variability). These data were tabulated where possible to enable cross-study comparison (e.g., nanosheet width/height vs. drive current; inner-spacer strategies vs. parasitic capacitance). Thematic synthesis was applied: papers were grouped into topics (historical evolution, device physics, fabrication/process challenges, industry implementation, future architectures and materials). For areas with conflicting results, the review reports both findings and notes differences in experimental conditions or simulation assumptions that may explain discrepancies.

Figures and schematics
Figures used in the manuscript are either (a) redrawn schematic diagrams based on primary sources (e.g., cross-sections of planar/FinFET/GAA, CFET stacking) to ensure clarity and consistent notation, or (b) original summary plots created from aggregated data in cited studies (with explicit attribution in captions). When a figure was adapted from a published source it is indicated in the caption and the original source is cited; permission steps are noted where required by the publisher.

Limitations and potential biases
This review is limited by public availability: many foundry process details remain proprietary and some claims (especially commercial PPA numbers) rely on vendor disclosures. Preprints and ResearchGate items were used selectively and flagged as such; they may later be revised. The search was restricted to English-language material. Finally, while the reference list is comprehensive for the stated timeframe (2008–2025), new advances occur rapidly—readers should consult the most recent conference proceedings (IEDM, VLSI) for the absolute latest experimental reports.

3. Discussion: Engineering the Future of Computing at 3nm

3.1. Device Physics: Overcoming the Physical Limits of FinFETs

3.1.1. FinFET's Scaling Hurdles at Sub-5nm Nodes

While FinFETs were a revolutionary solution for continuing Moore's Law for over a decade, their scaling to the sub-5nm regime revealed fundamental limitations [5]. At these ultra-scaled dimensions, FinFETs began to suffer from severe short-channel effects (SCE), Drain-Induced-Barrier-Lowering (DIBL), and quantum effects . Short-channel effects cause the transistor's electrical behavior to degrade as the gate length shrinks, leading to a loss of control over the channel . A particularly critical issue identified in device simulations is the quantum confinement effect . This phenomenon, which becomes significant when the fin width shrinks to just a few nanometers, causes a steep increase in the device's threshold voltage (Vth) . One study found that as the fin width shrinks from 5 nm to 4 nm, the Vth shift can reach 50 mV, prompting the conclusion that it is "reasonable to keep the fin width at 5 nm or greater" to avoid this effect . The ratio of the effective gate length to the fin thickness (Leff/Tfin) also emerges as a dominant factor limiting FinFET scalability . As this ratio falls below 1.5, DIBL and subthreshold swing (SS) increase abruptly, a clear sign of diminishing gate control . These physical problems in FinFETs demonstrate that their 3-sided gate was no longer an impregnable defense against leakage and performance degradation at these minuscule dimensions [6].

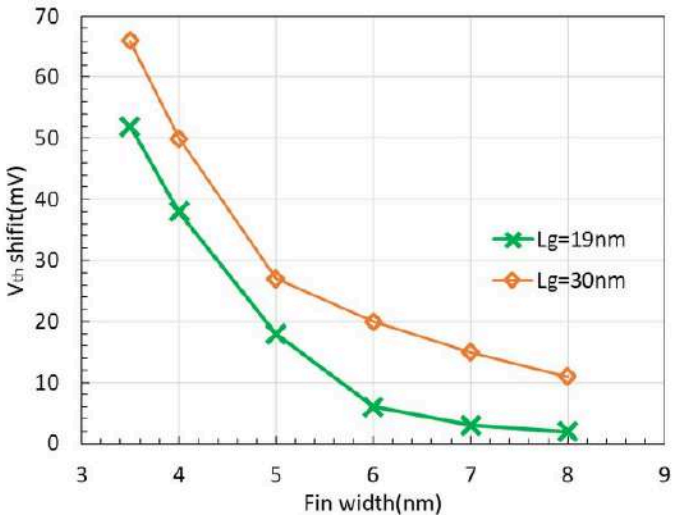

Figure 2. "Simulation results of threshold voltage shift by quantum confinement effect." Credits: The Effect of Fin Structure in 5 nm FinFET Technology, Journal of Microelectronic Manufacturing

3.1.2. The Superior Electrostatic Control of Gate-All-Around Transistors

The architectural shortcomings of FinFETs at scaled dimensions made the transition to GAA transistors a logical and necessary step. The core principle of a GAA transistor is its superior electrostatic control, achieved by enclosing the channel on all four sides with the gate [39] . This full "gated-all-around" design is the direct answer to the physical problems that plagued FinFETs at the 3nm node . By fully wrapping the channel, GAA transistors significantly mitigate

short-channel effects, reduce leakage current, and provide a lower threshold voltage . This increased control also results in a steeper subthreshold swing (SS), which is a key metric for transistor performance. A steeper SS allows for a more rapid transition between the ON and OFF states, enabling faster switching speeds and lower power consumption .

Beyond their fundamental physical advantages, nanosheet-based GAA designs, such as Samsung's MBCFET, introduce a crucial element of design flexibility [39] . Unlike the fixed, quantized nature of FinFETs where the drive current is restricted to multiples of the number of fins (one, two, or three), GAA nanosheets allow for the channel width to be varied [16]. This enables designers to precisely tune the transistor for an optimal balance of power and performance, a capability that is essential for a diverse range of modern applications, from ultra-low-power mobile devices to high-performance computing (HPC) processors . The improved electrostatic control and design flexibility of GAA transistors make them not just a solution to a specific scaling problem, but a foundational technology for a new era of semiconductor design.

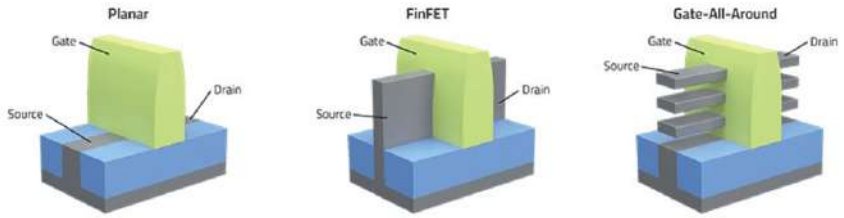

Figure 3. “Planar transistors vs. finFETs vs. gate-all-around Source” Credits: Lam Research

3.2. Fabrication Challenges: Beyond the FinFET Cliff

The transition to GAA transistors is not a single problem to be solved but a paradigm shift that introduces a new cascade of complex engineering and manufacturing challenges. The very design features that give GAA its performance benefits: stacked nanosheets and a fully enclosed gate also introduce new sources of process variability and manufacturing complexity that must be meticulously managed [39].

3.2.1. The Critical Role and Limitations of EUV Lithography

Extreme Ultraviolet (EUV) lithography is a critical technology for patterning at the 3nm node, but its implementation introduces significant costs and complexity . EUV light is absorbed by air and glass, necessitating the use of complex reflective optics in a vacuum . At ultra-scaled dimensions, EUV faces specific challenges, including stochastic effects that can cause line-edge roughness (LER) and a need for multi-patterning to achieve the required resolution . The advent of next-generation High Numerical Aperture (High-NA) EUV tools brings further complexity . These tools offer higher resolution but come with a significantly reduced depth of focus and a smaller field size due to anamorphic imaging . This necessitates a fundamental re-evaluation of chip design, requiring advanced techniques such as design stitching for larger dies or a shift toward a chiplet-based integration strategy .

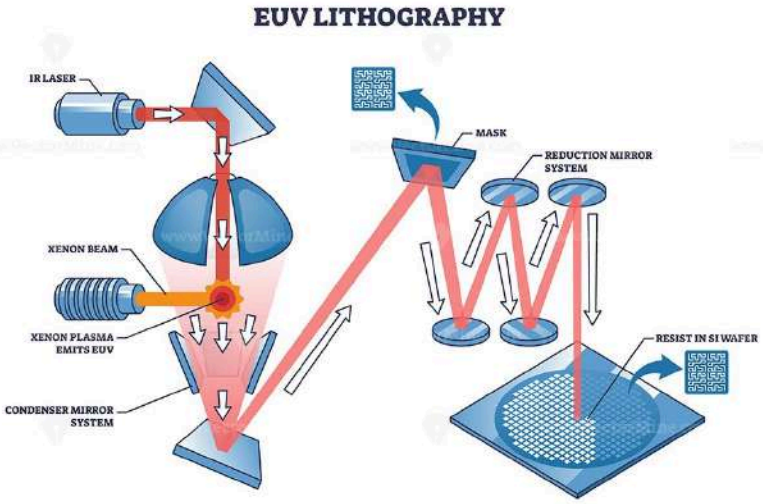

Figure 4. "EUV Lithography System" Credits: VectorMine

3.2.2. Inner Spacer Engineering and Parasitic Capacitance

The formation of inner spacers in GAA transistors is a multi-step process that is both complex and critical for device performance . The primary function of the inner spacer is to reduce parasitic capacitance, which can degrade the transistor's speed and efficiency . To achieve this, these spacers should ideally be made of low-κ (low dielectric constant) dielectric materials like silicon oxide (SiO2) [11]. However, these materials often lack the mechanical and thermal stability required to withstand the complex sequence of deposition and precise etching steps . A proposed solution to this dilemma is a hybrid dual-κ spacer strategy, which uses a more robust material like silicon nitride (Si3N4) for the inner spacers while using a low-κ material for the outer spacers [10]. This approach seeks to balance the conflicting requirements of low parasitic capacitance and material robustness, demonstrating the intricate nature of GAA fabrication [11].

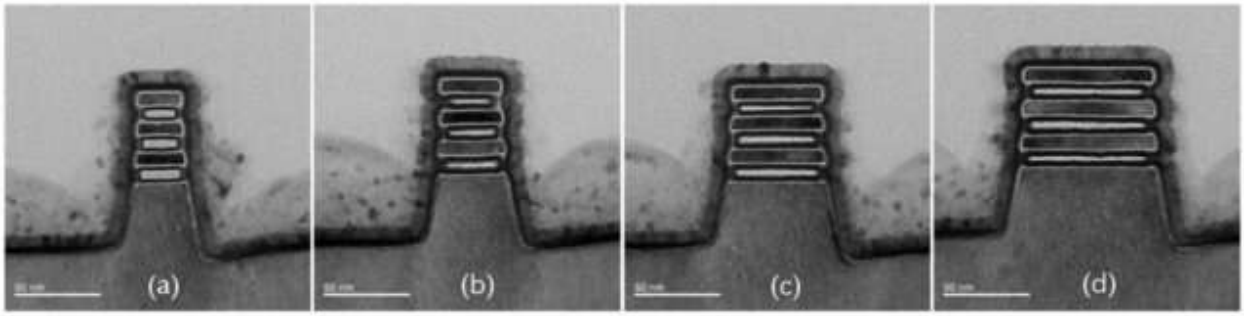

Figure 5. "TEM cross-sectional images of stacked nanosheets with multiple widths obtained by multi-step etching with the application of oxidation treatment. (a) 30 nm; (b) 40 nm; (c) 60 nm; (d) 80 nm." Credits: A Novel Si Nanosheet Channel Release Process for the Fabrication of Gate-All-Around Transistors and Its Mechanism Investigation, Nanomaterials (MDPI)

3.2.3. Nanosheet Stacking and Process Variability

The vertical stacking of multiple nanosheets, a core feature of GAA designs, introduces a new class of process variability challenges. Issues such as line-edge roughness (LER) and surface roughness scattering are particularly problematic for nanosheet and nanowire architectures, as they can significantly degrade device performance and carrier mobility . Maintaining consistent spacing between the stacked sheets is also critical, as unequal spacing can lead to variations in the threshold voltage (VT) . The sources collectively reveal that the very features that give GAA its performance benefits: the all-around gate and stacked channels also introduce new sources of process variability, parasitic capacitance, and manufacturing complexity [42]. The narrative of semiconductor manufacturing has shifted from simply shrinking dimensions to mastering the intricate, interlocking physical and chemical processes of three-dimensional integration.

3.3. Industry Implementation: A Comparative Analysis of Foundry Strategies

The strategic choices of the leading foundries at the 3nm node provide a vivid illustration of the complex interplay between technological innovation and market dynamics. The decision to adopt a new architecture is deeply intertwined with a company's market position and risk tolerance.

3.3.1. Samsung's Early GAA Gamble

Samsung made a bold, high-risk move by being the first to announce and begin production of its 3nm GAA process (3GAE) in mid-2022 [48] . The company's proprietary MBCFET architecture, which uses nanosheets, was a deliberate step to defy the performance limitations of FinFETs . Samsung's first-generation 3nm process delivered significant PPA gains over its 5nm process, achieving up to a 45% reduction in power consumption, a 23% improvement in performance, and a 16% reduction in area . Despite initial reports of low yields (10-20%), the company later claimed to have achieved a "perfect level" suitable for mass production . Samsung's strategy was a high-risk, high-reward approach to gain a competitive edge and attract customers, a move that positioned it as an innovator despite the initial manufacturing complexities .

Figure 6. “3nm GAA Technology” Credits: Samsung

3.3.2. TSMC's Last FinFET Stand

In contrast to Samsung, TSMC pursued a more conservative strategy, producing its 3nm process (N3/N3E) using a highly refined FinFET architecture [8] . The N3 process offers a 10-15% increase in performance or a 25-35% decrease in power consumption, along with a significant 70% increase in logic density over its 5nm node . TSMC's FinFlex technology is a notable innovation within this node, allowing for the intermixing of cells with different numbers of fins to optimize for specific PPA points . However, this strategic choice was made with the clear understanding that the FinFET architecture had reached its fundamental limits [6]. Experts from IEDM 2022 noted that after the implementation of features like FinFlex, "there will be no more room left for improvement of FinFET-based process technologies" [41] . TSMC's decision to stick with FinFET for its 3nm node was a strategic move to extract the final gains from a mature technology before its inevitable transition to nanosheet-based GAA technology at the 2nm node [5] .

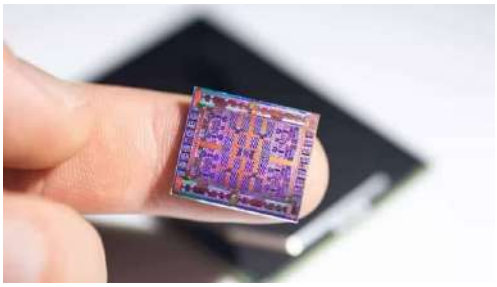

Figure 7. “TSMC 3nm FinFet Technology.” Credits: TSMC

3.3.3. Intel's Strategic Leapfrog

Intel, facing a significant gap in manufacturing leadership, is betting on a long-term strategy to leapfrog its competitors . Its roadmap is centered on the 18A node, which is set for high-volume production by 2025 . This node is distinguished by two major innovations: RibbonFET, Intel's GAA implementation, and PowerVia, an industry-first backside power delivery network . Intel claims that RibbonFET alone offers up to a 15% improvement in performance per watt compared to its FinFETs, while PowerVia can further boost performance by 4% and improve cell utilization by 5-10% by separating power and signal pathways [8]. By integrating two major architectural shifts at once a new transistor and a new power delivery system Intel aims to reclaim its former position of process leadership .

The quantitative differences between these strategies are a key indicator of their underlying design philosophies. The following table consolidates key PPA metrics and other data points for a clear comparison.

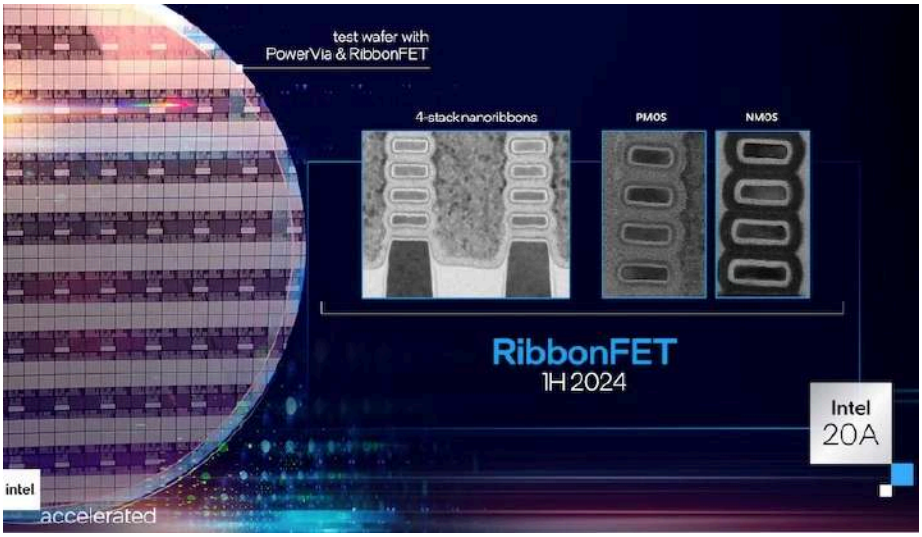

Figure 8. “Intel (RibbonFET, 18A)” Credits: Intel

Foundry	Process Name	Transistor Type	Transistor Density (MTr/mm²)	Performance Gain (%)	Power Reduction (%)	Area Reduction (%)	Release Status
Samsung	3GAE	MBCFET (GAA)	150	23% (vs. 5nm)	45% (vs. 5nm)	16% (vs. 5nm)	2022 (first shipment)
TSMC	N3	FinFET	197	10-15% (vs. N5)	25-35% (vs. N5)	70% (logic)	2022 (volume production)
TSMC	N3E	FinFET	190	10-15% (vs. N5)	30-35% (vs. N5)	N/A (FinFlex dependent)	2023 (H1 shipping)
Intel	18A	Ribbon	190	15%	N/A	N/A	2025

	(projected)	FET (GAA)	(estimated)	(per watt vs. FinFETs)			(H2 production)

3.4. The Future of Ultra-Scaled Technology Beyond 3nm

The roadmap for semiconductor technology beyond 3nm is no longer a simple, linear progression. The industry is moving toward a multi-pronged, multi-disciplinary approach to sustain the pace of innovation.

3.4.1. Next-Generation Architectures: Forksheets and CFETs

As GAA nanosheets approach their own physical limits, new architectures are already being explored [16]. A key successor is the Complementary Field-Effect Transistor (CFET), which stacks nMOS and pMOS devices vertically . This approach promises to achieve a potential 50% area reduction in standard cells by eliminating the need for n-to-p separation on the die . The manufacturing techniques developed for GAA, such as nanosheet stacking, will directly inform the transition to CFETs, which can be viewed as the next logical step in vertical integration [39].

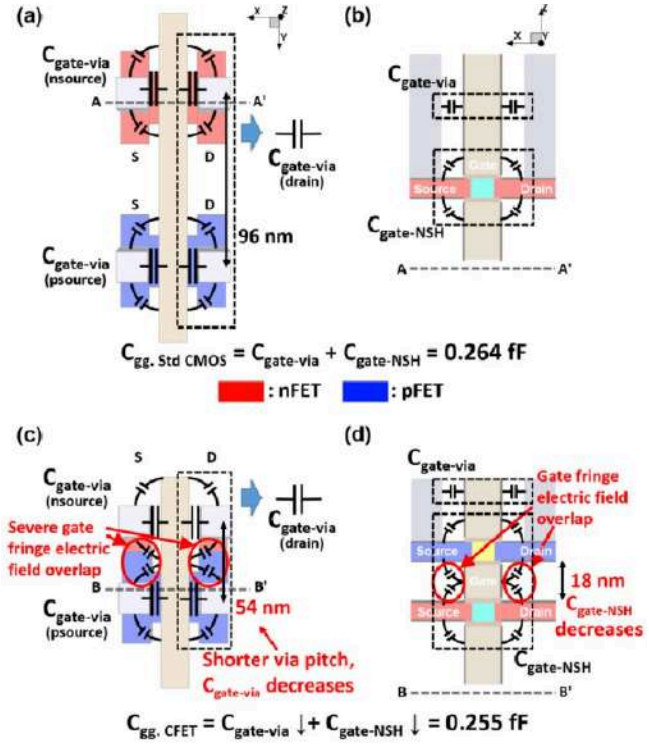

Figure 9. "(a) Top view and (b) cross-sectional view of standard CMOS structure with schematic of capacitive component. (c) Top view and (d) cross-sectional view of default CFET structure with schematic of capacitive component." Credits: Performance Analysis on Complementary

FET (CFET) Relative to Standard CMOS with Nanosheet FET, IEEE Journal of the Electron Devices Society

3.4.2. Novel Materials: The Search for a Post-Silicon Paradigm

As silicon approaches its fundamental physical limits, the search for a post-silicon material has intensified . Two-dimensional (2D) semiconductors, such as indium selenide (InSe) and molybdenum disulphide (MoS2), are promising candidates due to their superior electrical properties and atomic-scale thinness . InSe transistors, for example, have demonstrated electron mobility up to 287 $cm^2/V \cdot s$, outperforming ultra-thin silicon and achieving a near-ideal subthreshold swing . While these materials show immense promise, a major engineering challenge remains the fabrication of high-quality, uniform wafers at an industrial scale.

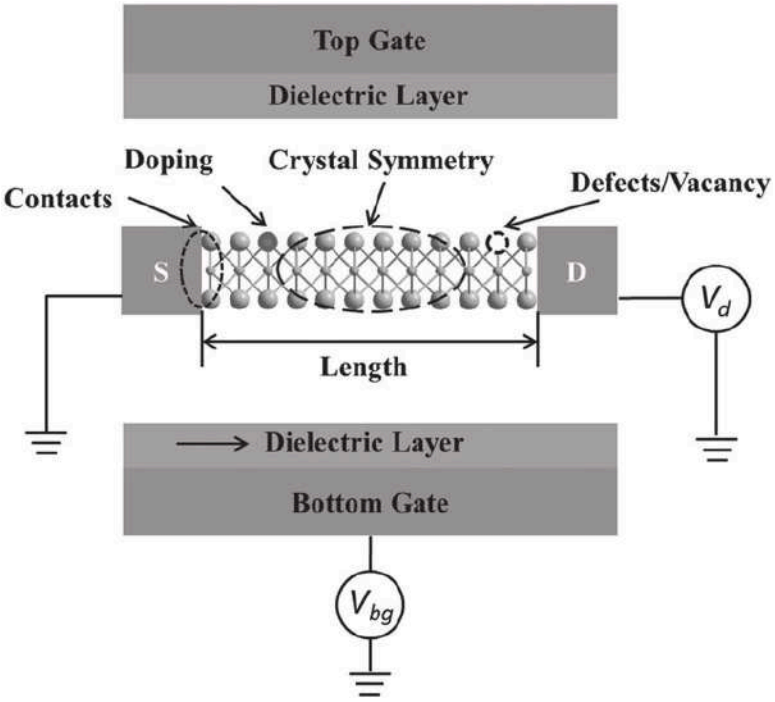

Figure 10. “Scheme of a typical FET device based on 2D layered semiconducting materials.” Credits: Progress on Electronic and Optoelectronic Devices of 2D Layered Semiconducting Materials, ResearchGate

3.4.3. The Influence of AI Hardware in Driving Innovation

The voracious demands of modern artificial intelligence and machine learning (AI/ML) workloads are profoundly influencing the direction of semiconductor technology . These workloads require immense computational power, massive memory capacity, and low latency, straining the

traditional model of scaling . The industry has responded by shifting focus from purely transistor-level scaling to a more holistic, system-level approach . Specialized architectures like GPUs and Wafer-Scale Engines (WSEs) are now the workhorses of AI, relying on innovations in parallel processing and advanced packaging to deliver performance gains that are no longer achievable through simple density increases . GAA transistors are a key enabler of this trend, as their enhanced performance per watt and superior scalability are ideal for AI accelerators and other HPC applications . The fact that GAA technology allows for more compute power in the same footprint with lower power is a direct answer to the power and heat challenges of modern AI hardware .

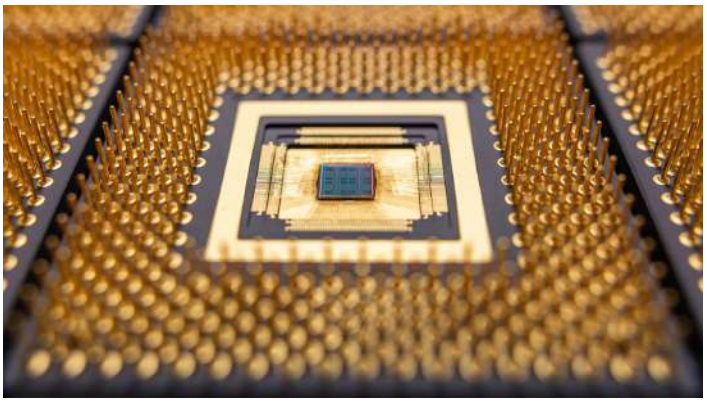

Figure 11. “AI-focused chip for enhanced computational performance in AI workloads. ” Credits: Princeton Engineering

3.4.4. Challenges in SRAM Scaling and Stability

A compelling piece of evidence for the shift away from linear scaling is the challenge of scaling static random-access memory (SRAM) . As transistors shrink, SRAM cells become highly susceptible to process-induced variations, making it difficult to maintain stability at scaled voltages . While IBM has demonstrated a 3nm nanosheet SRAM cell, TSMC's 3nm FinFET process saw little to no shrinkage in its SRAM cell area [6]. This indicates that SRAM is no longer scaling at the same rate as logic transistors and now accounts for a larger portion of the die . This failure of SRAM to scale in tandem with logic transistors highlights the end of the traditional, uniform scaling paradigm and reinforces the need for architectural and packaging innovations like chiplets to optimize entire systems rather than just individual components .

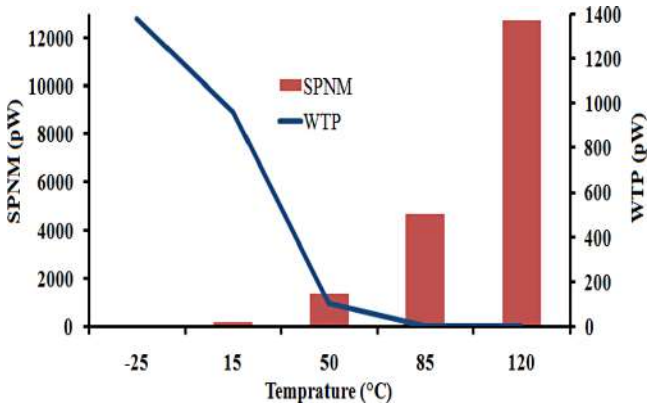

Figure 12. "Stability of CNTFET 6T SRAM Cell" Credits: Springer Nature Link

4. Conclusion

The 3nm node represents a critical inflection point in the semiconductor industry, marking the end of the FinFET era and the definitive arrival of the Gate-All-Around (GAA) transistor. The transition was not arbitrary but a necessary response to the fundamental physical limitations that FinFETs could no longer overcome, including severe short-channel effects and quantum confinement phenomena that plagued performance at ultra-scaled dimensions. By fully enclosing the channel, GAA transistors provide the superior electrostatic control required to mitigate these issues, offering significant gains in power efficiency, performance, and density.

The implementation of GAA technology, however, introduces a new class of complex engineering challenges. The intricate processes of advanced EUV lithography, inner spacer engineering, and nanosheet stacking demand a holistic, multidisciplinary approach to manufacturing [40]. The divergent strategies of leading foundries Samsung's early gamble versus TSMC's last stand with FinFET demonstrate how these technological decisions are deeply intertwined with market position and risk tolerance.

Looking beyond 3nm, the future of ultra-scaled semiconductor technology is not defined by a single metric or a single material. Instead, it is a complex, symbiotic ecosystem of innovation across multiple fronts: new architectures like CFETs, the long-term search for a post-silicon material, and system-level co-optimization driven by the voracious demands of AI hardware. The failure of key components like SRAM to scale at the same pace as logic transistors is the most compelling evidence of this shift. As a result, the industry must now rely on ingenuity and innovation across the entire computing stack, from the device level to the system level, to continue the progress predicted by Moore's Law into the Angstrom Era [35].

References

1. ASML. (2022). *What is a gate-all-around transistor?* ASML. https://www.asml.com/en/news/stories/2022/what-is-a-gate-all-around-transistor

2. Anonymous. (2023). *Introduction of gate-all-around FET (GAAFET).* ResearchGate. https://www.researchgate.net/publication/376672940_Introduction_of_Gate-All-Around_F

ET_GAAFET

3. Intel. (2023). *Moore's Law.* Intel Newsroom. https://newsroom.intel.com/press-kit/moores-law

4. IMEC. (2023). *Is Moore's Law dead?* IMEC. https://www.imec-int.com/en/semiconductor-education-and-workforce-development/microchips/moores-law/moores-law-dead

5. Anonymous. (2020). *The effect of fin structure in 5 nm FinFET technology.* ResearchGate. https://www.researchgate.net/publication/338338449_The_Effect_of_Fin_Structure_in_5_nm_FinFET_Technology

6. JoMM. (2019). *The effect of fin structure in 5 nm FinFET technology.* Journal of Microelectronic Manufacturing. http://www.jommpublish.org/static/publish/FD/A5/3C/FD22E94A56A6F248835F13A5A9/10.33079.jomm.19020405.pdf

7. MDPI. (2023). *A comparative study of the effects of different doping profiles on the performance of junctionless cylindrical surrounding gate MOSFETs with ultrascaled dimensions. Micromachines, 15*(4), 424. https://www.mdpi.com/2072-666X/15/4/424

8. Cronfa Swansea. (2020). *Benchmarking of FinFET, nanosheet, and nanowire FET architectures for future technology nodes.* Swansea University. https://cronfa.swan.ac.uk/Record/cronfa53939/Download/53939__17053__639075c9775a4e0098bed8791269586c.pdf

9. Anysilicon. (2023). *The ultimate guide to gate-all-around (GAA).* AnySilicon. https://anysilicon.com/the-ultimate-guide-to-gate-all-around-gaa/

10. Google Patents. (2021). *Inner spacer feature with porous dielectric material* (US20210083091A1). https://patents.google.com/patent/US20210083091A1/en

11. Anonymous. (2020). *Hybrid dual-κ spacer strategy to optimize parasitic capacitance and driving performance in GAA nanosheet FETs.* ResearchGate. https://www.researchgate.net/figure/Spacer-morphology-and-inner-spacer-process-challenges-a-conventional-spacer-b-inner_fig2_340841753

12. Samsung. (2022). *Samsung begins chip production using 3nm process technology with GAA architecture.* Samsung Newsroom. https://news.samsung.com/global/samsung-begins-chip-production-using-3nm-process-technology-with-gaa-architecture

13. Samsung. (2024). *Foundry process technology.* Samsung Semiconductor. https://semiconductor.samsung.com/foundry/process-technology/logic-node/

14. Semiconductor Digest. (2018, May). *EUV lithography: Extending the patterning roadmap to 3nm.* Semiconductor Digest. https://sst.semiconductor-digest.com/2018/05/ultra-violet-lithography-extending-the-patterning-roadmap-to-3nm/

15. Anonymous. (2024). *Simulation of vertically stacked 2-D nanosheet FETs.* ResearchGate. https://www.researchgate.net/publication/388786072_Simulation_of_Vertically_Stacked_2-D_Nanosheet_FETs

16. MDPI. (2022). *A detailed comparison of channel width folding for FinFET, vertically stacked nanosheet and nanowire transistors. Nanomaterials, 12*(10), 1739. https://www.mdpi.com/2079-4991/12/10/1739

17. PatentPC. (2024). *5nm vs. 3nm chips: Performance gains and market adoption rates.* PatentPC. https://patentpc.com/blog/5nm-vs-3nm-chips-performance-gains-and-market-adoption-rates-latest-data

18. Samsung. (2022). *Samsung begins chip production using 3nm process technology with GAA architecture.* Samsung Newsroom. https://news.samsung.com/global/samsung-begins-chip-production-using-3nm-process-technology-with-gaa-architecture

19. SemiWiki. (2023). *Intel 18A node explained: How RibbonFET boosts AI scalability.* SemiWiki. https://semiwiki.com/forum/threads/intel-18a-node-explained-how-ribbonfet-boosts-ai-scalability.21352/

20. GameGPU. (2024). *Intel reveals all tech details 18A — its flagship 1.8 nm class process technology.* GameGPU. https://en.gamegpu.com/iron/intel-reveals-all-tech-details-18a-power-via-ribbonfet-and-30-graphics

21. USPTO. (2019). *8T-SRAM cell scaling beyond 10 nm technology.* U.S. Patent and Trademark Office. https://ptacts.uspto.gov/...

22. SemiEngineering. (2025). *SRAM with mixed signal logic with noise immunity in 3nm nanosheet (IBM).* SemiEngineering. https://semiengineering.com/sram-with-mixed-signal-logic-with-noise-immunity-in-3nm-nanosheet-ibm/

23. PatentPC. (2024). *Samsung vs. TSMC vs. Intel: Who's winning the foundry market.* PatentPC. https://patentpc.com/blog/samsung-vs-tsmc-vs-intel-whos-winning-the-foundry-market-latest-numbers

24. TSMC. (2025). *3nm technology.* TSMC. https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_3nm

25. Cadence. (2022). *IEDM: TSMC N3 details.* Cadence Breakfast Bytes Blog. https://community.cadence.com/cadence_blogs_8/b/breakfast-bytes/posts/iedm-tsmc-n3-details

26. SemiWiki. (2023). *Samsung 3nm process technology wiki.* SemiWiki. https://semiwiki.com/wikis/industry-wikis/samsung-3nm-process-technology-wiki/

27. Intel. (2025). *Intel 18A process technology simply explained.* Intel Newsroom. https://newsroom.intel.com/intel-foundry/intel-18a-process-technology-simply-explained

28. Electropages. (2024). *Intel 18A: The future of semiconductor technology with RibbonFET and PowerVia.* Electropages. https://www.electropages.com/blog/2024/10/intel-18a-future-semiconductor-technology-ribbonfet-and-powervia

29. Semiconductor Digest. (2024). *The shape of tomorrow's semiconductor technology.* Semiconductor Digest. https://www.semiconductor-digest.com/the-shape-of-tomorrows-semiconductor-technology/

30. Atomfair. (2024). *The post-FinFET era: Exploring the design and scaling of Gate-All-Around (GAA) nanosheet transistors.* Atomfair. https://atomfair.com/scibase2/article.php?id=40

31. Future Timeline. (2025). *First wafer-scale fabrication of 2D indium selenide semiconductors.* Future Timeline. https://www.futuretimeline.net/blog/2025/08/6-first-wafer-scale-fabrication-2d-indium-selenide-semiconductors.htm

32. Prescouter. (2024). *Roadmap to integrating 2D materials for next-gen electronics.* Prescouter. https://www.prescouter.com/2024/07/roadmap-to-integrating-2d-materials/

33. ArXiv. (2025). *A comprehensive analysis and comparison of the wafer-scale engine and Nvidia's GPU architecture for AI acceleration.* arXiv. https://arxiv.org/html/2503.11698v1

34. Anonymous. (2024). *Exploring the synergy of AI and ML in very large scale integration design and manufacturing.* ResearchGate. https://www.researchgate.net/publication/386302071_Exploring_the_synergy_AI_and_M

L_in_very_large_scale_integration_design_and_manufacturing

35. MIT CSAIL. (2024). *The death of Moore's Law: What it means and what might fill the gap going forward.* MIT CSAIL. https://cap.csail.mit.edu/death-moores-law-what-it-means-and-what-might-fill-gap-going-forward

36. Anonymous. (2021). *Comparison of FinFET, GAA nanowire, and nanosheet FET architectures for sub-10 nm nodes.* ResearchGate. https://www.researchgate.net/figure/Comparison-of-a-FinFET-b-vertically-stacked-nanosheet-GAA-FET-and-c-vertically_fig1_360743373

37. Chinese Journal of Semiconductors. (2008). *Analysis and TCAD simulation of a gate-all-around cylindrical FinFET.* Chinese Journal of Semiconductors. https://www.jos.ac.cn/fileBDTXB/oldPDF/08070503.pdf

38. Anonymous. (2018). *Gate-all-around silicon nanowire field-effect transistors for ultimate CMOS scaling.* ResearchGate. https://www.researchgate.net/figure/TCAD-simulation-results-of-a-the-carriers-density-and-b-electric-field-profiles-for_fig10_326815579

39. MDPI. (2023). *SnO nanosheet transistor with remarkably high hole effective mobility. Nanomaterials, 15*(9), 640. https://www.mdpi.com/2079-4991/15/9/640

40. Anonymous. (2021). *Review on fabrication and simulation of nano-sheet transistors.* ResearchGate. https://www.researchgate.net/figure/Schematic-diagrams-for-NSFET-fabrication-47_fig3_351590703

41. Anonymous. (2018). *FinFET versus gate-all-around nanowire FET: Performance scaling and variability.* ResearchGate. https://www.researchgate.net/publication/323090508_FinFET_versus_Gate-All-Around_Nanowire_FET_Performance_Scaling_and_Variability

42. SPIE. (2024). *A survey of structural design and performance impacts of GAA MBCFET. Proceedings of SPIE, 13547*, 1354729. https://www.spiedigitallibrary.org/conference-proceedings-of-spie/13547/1354729

43. Anonymous. (2018). *FinFET versus gate-all-around nanowire FET: Performance scaling and variability.* ResearchGate. https://www.researchgate.net/publication/323090508_FinFET_versus_Gate-All-Around_Nanowire_FET_Performance_Scaling_and_Variability

44. Anonymous. (2011). *Short-channel effects in double-gate FinFETs.* ResearchGate. https://www.researchgate.net/figure/Short-Channel-Effects-variation-with-L-T-fin-ratio_fig

1_50848469

45. ArXiv. (2020). *Negative capacitance enables FinFET scaling beyond 3nm node.* arXiv. https://arxiv.org/pdf/2007.14448

46. TechInsights. (2022). *TSMC reveals 3nm process details.* TechInsights. https://www.techinsights.com/blog/tsmc-reveals-3nm-process-details

47. Patsnap. (2024). *Integrating GAA-based logic gates for computation in ELMs.* Patsnap. https://eureka.patsnap.com/report-integrating-gaa-based-logic-gates-for-computation-in-elms

48. Anonymous. (2019). *3nm GAA technology featuring multi-bridge-channel FET for low power and high performance applications.* ResearchGate. https://www.researchgate.net/publication/330589929_3nm_GAA_Technology_featuring_Multi-Bridge-Channel_FET_for_Low_Power_and_High_Performance_Applications

49. IEDM. (2023). *EUV driven GAA scaling.* IEEE IEDM. https://www.mapyourshow.com/mys_shared/iedm23/handouts/2-3_Mon_16241.pdf

50. WikiChip. (2022). *TSMC N3 and challenges ahead.* WikiChip Fuse. https://fuse.wikichip.org/news/7375/tsmc-n3-and-challenges-ahead/

51. TechInsights. (2022). *TSMC reveals 3nm process details.* TechInsights. https://www.techinsights.com/blog/tsmc-reveals-3nm-process-details

52. SemiWiki. (2022). *IEDM 2022: TSMC 3nm.* SemiWiki. https://semiwiki.com/semiconductor-manufacturers/tsmc/322688-iedm-2022-tsmc-3nm/

53. VKTR. (2024). *The end of Moore's Law? AI chipmakers say it's already happened.* VKTR. https://www.vktr.com/ai-technology/the-end-of-moores-law-ai-chipmakers-say-its-already-happened/

54. Asterisk Magazine. (2024). *The transistor cliff.* Asterisk Magazine. https://asteriskmag.com/issues/03/the-transistor-cliff

55. GM Insights. (2024). *Gate-all-around (GAA) transistor market size, share, trends & forecast.* GM Insights. https://www.gminsights.com/industry-analysis/gate-all-around-gaa-transistor-market

56. Future Timeline. (2025). *First wafer-scale fabrication of 2D indium selenide semiconductors.* Future Timeline. https://www.futuretimeline.net/blog/2025/08/6-first-wafer-scale-fabrication-2d-indium-selenide-semiconductors.htm

57. MDPI. (2023). *A breakthrough in the batch production of wafer-scale monolayer MoS_2 by chemical vapor deposition. Crystals, 13*(8), 1275. https://www.mdpi.com/2073-4352/13/8/1275

58. NCBI. (2022). *Wafer-scale synthesis of 2D MoS_2 for next-generation integrated electronics. Nature Communications, 13*(1), 435. https://pmc.ncbi.nlm.nih.gov/articles/PMC9419721/